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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,597	08/29/2003	Yang Ping Lim	10021207-1	8909

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EXAMINER	
LAM, HUNG H	

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2622	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/651,597	LIM ET AL.	
	Examiner	Art Unit	
	Hung H. Lam	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendments, filed on 08/06/07, have been entered and made of record. Claim 19 is added. Claims 1-19 are pending.

Response to Arguments

2. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-2, 4-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Boemler (US-6,965,407).

With regarding **claim 1**, Boemler discloses an imaging system comprising:

an array of pixel sensors (Figs. 3 and 8; pixels 12);

a first bank of sample-and-hold circuits connected to the pixel sensors (Figs. 3 and 8; latch 124 and 24b; Col. 6, Ln. 45-67);

a second bank of sample-and-hold circuits connected to the pixel sensors (Figs. 3 and 8; latch 24 and 24a; Col. 6, Ln. 45-67);

a first analog-to-digital converter (Figs. 3; see ADC_COLL and BK_COLL);

a second analog-to-digital converter (Figs. 3; see ADC_COLL and BK_COLL); and

a selection circuit (Figs. 3 and 8; see the switches in ADC_COLL, BK_COLL and DQ latch) operable to select and connect a sample-and-hold circuit from the first bank to the first analog-to-digital converter and simultaneously select and connect a sample-and-hold circuit from the second bank to the second analog-to-digital converter (Col. 6, Ln. 45-Col. 7, Ln. 36; Col. 8, Ln. 1-28).

wherein the sample-and-hold circuit from the first bank is selectively connected to a row of the array for sampling a succession of reset voltages only from corresponding columns of the selected row (Fig. 3; Col. 6, Ln. 45-67; Col. 8, Ln. 1-28), and

the sample-and-hold circuit from the second bank of the array is selectively connected to the same row of the array for sampling a succession of integrated voltages only from the corresponding columns of the same selected row (Col. 6, Ln. 45-67; Col. 8, Ln. 1-28).

With regarding **claim 2**, Boemler discloses the imaging system wherein the array includes a plurality of columns of the pixel sensors (12), and columns of pixel sensors are connected to respective sample-and-hold circuits in the first bank and to respective sample-and-hold circuits in the second bank (see Figs. 3).

With regarding **claim 4**, Boemler discloses the system further comprising a control circuit that activates the first bank to sample reset voltages in a first selected set of pixel sensors and activates the second bank to sample integrated voltages in a second selected set of pixel sensors (abstract; Col. 6, Ln. 45-67).

With regarding **claim 5**, Boemler discloses the system wherein the first selected set of pixel sensors consists of the pixel sensors that are in a row of the array that has just been reset (abstract; Col. 6, Ln. 45-67).

With regarding **claim 6**, Boemler discloses the system wherein the first selected set of pixel sensors consists of the pixel sensors that are in a row of the array for which an exposure time has lapsed since a last reset of the row (abstract; Col. 6, Ln. 45-Col. 7, Ln. 35).

With regarding **claim 7**, Boemler discloses the system wherein:

the selection circuit is operable in a digital correlated double sampling mode (abstract), wherein the selection circuit connects a selected sample-and-hold circuit from the first bank to the first analog-to-digital converter and simultaneously connects a selected sample-and-hold circuit from the second bank to the second analog-to-digital converter (abstract; Col. 6, Ln. 45-67); and

the selection circuit is operable in an analog correlated double sampling mode (abstract), wherein the selection circuit simultaneously connects the selected sample-and-hold circuit from the first bank and the selected sample-and-hold circuit from the second bank to one of the first analog-to-digital converter and the second analog-to-digital converter (abstract; Col. 6, Ln. 45-67).

With regarding **claim 8**, Boemler discloses an imaging method comprising:

(a) resetting selected pixel sensors in an image sensor (abstract; Col. 6, Ln. 45-67);

(b) sampling reset voltages of the selected pixel sensors (Col. 6, Ln. 45-67);

(c) converting the reset voltages to digital reset values using a first channel (Col. 6, Ln. 45-67);

(d) sampling integrated voltage of the selected pixel sensors after lapse of an exposure time (Col. 6, Ln. 45-Col. 7, Ln. 36);

(e) converting the integrated voltages to digital integrated values using a second channel (Figs. 3; see ADC_COLL and BK_COLL)

(f) changing which pixel sensors in the image sensor are the selected pixel sensors (Col. 6, Ln. 66-Col. 7, Ln. 19); and

(g) repeating steps (a) to (f), wherein converting the integrated voltages overlaps with converting the reset voltage (Col. 6, Ln. 66-Col. 7, Ln. 36).

sampling the reset voltages is performed by the first channel only and sampling the integrated voltage is performed by the second channel only (Col. 6, Ln. 45-67).

With regarding **claim 9**, Boemler discloses the method wherein converting the integrated voltages for pixel sensors overlaps with converting the reset voltage for other pixel sensors (Col. 6, Ln. 45-67; Col. 8, Ln. 1-28).

With regarding **claim 10**, Boemler discloses the method wherein converting the integrated voltages for pixel sensors that are capturing a first frame of a moving image overlaps with converting the reset voltage for other pixel sensors that are capturing a second frame of the moving image (Col. 8, Ln. 1-28).

With regarding **claim 11**, Boemler discloses the method wherein repetitions of step (c) provide a continuous stream of the digital reset values including digital reset values for the first frame and the second frame (Col. 6, Ln. 66-Col. 7, Ln. 36; Col. 4, Ln. 45-67).

With regarding **claim 12**, Boemler discloses the method wherein repetitions of step (e) provide a continuous stream of the digital integrated values including digital integrated values for the first frame and the second frame (abstract; Col. 6, Ln. 66-Col. 7, Ln. 36; Col. 4, Ln. 45-67).

With regarding **claim 13**, Boemler discloses the method wherein repetitions of step (c) are separated by a time Tout, and each repetition of step (e) follows a corresponding repetition of step (c) by a time Texp (Col. 6, Ln. 66-Col. 8, Ln. 39).

With regarding **claim 14**, Boemler discloses the method wherein the time Tout is about equal to a required time for output digital values corresponding to a row of the pixel sensors (Col. 6, Ln. 66-Col. 8, Ln. 39).

With regarding **claim 15,** Boemler discloses the method wherein the time Texp is about equal to an exposure time for an image (Col. 6, Ln. 66-Col. 8, Ln. 39).

With regarding **claim 16,** Boemler discloses the method wherein the first channel comprises a first analog-to-digital converter, and the second channel comprises a second analog-to-digital converter (Figs. 3; see ADC_COLL and BK_COLL).

With regarding **claim 17,** Boemler discloses the method wherein repetitions of step (c) provide a continuous stream of the digital reset values (abstract; Col. 3, Ln. 15-30; Col. 4, Ln. 50-Col. 5, Ln. 7).

With regarding **claim 18,** Boemler discloses the method wherein repetitions of step (e) provide a continuous stream of the digital integrated values (abstract; Col. 6, Ln. 66-Col. 8, Ln. 39).

With regarding **claim 19,** Boemler discloses the system of claim 1, wherein the succession of reset voltages and the succession of integrated voltages are configured for simultaneous sampling of the selected row by the sample-and-hold circuit from the first and second banks, respectively (abstract; Col. 6, Ln. 66-Col. 8, Ln. 39).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boemler.

With regarding **claim 3**, Boemler discloses the system further comprising:

a buffer (Fig. 3; bus 128 and 28 are broadly interpreted as a buffer) coupled to receive a digital output signal from the first analog-to-digital converter (Fig. 3; A/D 40i-n); and

an adder coupled to determine a difference between a digital output signal from the buffer and a digital output signal from the second analog-to-digital converter (Fig. 3; subtract or 32; abstract; Col. 6, Ln. 60-Col. 7, Ln. 19).

However, Boemler fails to explicitly disclose a buffer/ memory register is a FIFO form.

Official Notice is taken that it is well known and expected in the art to implement a FIFO form into a buffer or memory register for reducing memory size. Therefore, it would have been obvious to one of ordinary skill in the art to modify the device of Boemler and Nakamura to include a FIFO buffer or register. The modifications thus reduce memory size and cost.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Ewedemi (US-6,831,684) discloses a digital correlating double memory circuit.

b) Borg(US-6,476,864) discloses a pixel sensor architecture outputting integrated and reset signals in different outputs.

c) Kang (US-2004/0,268,006) discloses an ECP bus having an internal buffer and supporting DMA transfer and data compression.

d) Vinnakota (US-2004/0,010,650) discloses a bus architecture wherein the internal interface buffers network data between the internal bus and the external bus architecture.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung H. Lam whose telephone number is 571-272-7367. The examiner can normally be reached on Monday - Friday 8AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, LIN YE can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HL
10/15/07

LIN YE
SUPERVISORY PATENT EXAMINER